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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,245	10/27/2003	James F. Orsillo	6427-65559	4337

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,245	ORSILLO, JAMES F.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *43* is/are allowed.

6)☒ Claim(s) *1-3,6,8-11,14-16,23-40 and 42* is/are rejected.

7)☒ Claim(s) *4,5,7,12,13,17-22 and 41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/04, 10/03*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 2, filed April 13, 205, with respect to claims 1-43 have been fully considered and are persuasive. The restriction requirements of claims 1-43 have been withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 6, 8-11, 14-16, 23-40 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakajima et al (5804983).

Regarding claim 1, Nakajima et al disclose [see Figs. 1, 3 and 9] an assembly for testing semiconductor devices (semiconductor wafer 14) with a probe station (probe apparatus 11), the probe station (11) having a head stage (head plate 17), the assembly comprising: a first plate (probe unit 21) configured to be mounted to and completely removable from the head stage (17) of the probe station (11), a second plate (ring plate 18) configured to be removably coupled to the first plate (21), the second plate (18) having a major aperture for receiving a probe-card assembly (probe card holder 25 and probe card 22) and first and second, opposed major surfaces; and docking equipment (ball hinge mechanism 52) mounted to the second plate (18) to facilitate docking of a tester (tester 28) to the probe station (11).

Regarding claim 2, Nakajima et al disclose at least one adjustment mechanism (adjustment screw mechanism 53) configured to adjust the tilt orientation of the probe-card assembly (25 with 22) [via ring 18] relative to the head stage (17).

Regarding claim 3, Nakajima et al disclose the at least one adjustment mechanism (53) comprises an adjusting screw (manual adjustment screw 53a) extending through the plate (18) and bearing against an adjacent surface of the head stage (17), wherein adjustment of the adjusting screw (53a) changes the tilt orientation of the first plate (21), the second plate (18), and the probe-card assembly (25 with 22) relative to the head stage (17).

Regarding claim 6, Nakajima et al disclose the second plate (18) comprises a lip portion [not number but shown] circumscribing the major aperture for supporting the probe-card assembly (25 with 22).

Regarding claim 8, Nakajima et al disclose the head stage (17) defines a head stage major aperture; the first plate (21) is formed with a first plate major aperture and a recessed portion substantially surrounding the first plate major aperture; and the second plate (18) is configured to fit within the recessed portion of the first plate (21) such that whenever the second plate (18) is positioned in the recessed portion, the major aperture of the second plate (18) at least partially overlaps the first plate major aperture and the head stage major aperture (17), thereby allowing a probe card (probe card 22) of the probe-card assembly (25 with 22) to contact a semiconductor device (semiconductor wafer 14) in the probe station (11).

Regarding claim 9, Nakajima et al disclose at least one alignment pin (not number but shown in Fig. 3) extending from one of the first (21) and second (18) plates and a pin hole (not number but shown in Fig. 3) for receiving the alignment pin formed in the other of the first (21)

and second (18) plates, the alignment pin and pin hole facilitating alignment of the second plate (18) relative to the first plate (21).

Regarding claim 10, Nakajima et al disclose whenever the second plate (18) is positioned in the recessed portion of the first plate (21), an upper surface of the first plate (21) is generally co-planar with an upper surface of the second plate (18).

Regarding claim 11, Nakajima et al disclose the major aperture of the second plate (18) is dimensioned to receive a probe-card assembly (25 with 22) having a first diameter; and the assembly (25 with 22) further comprises a third plate (contact ring 26) for mounting to the head stage (17) when the first (21) and second (18) plate are not mounted to the head stage (17), the third plate (26) being completely removable from the head stage (17) and having a major aperture for receiving a probe-card assembly (25 with 22) having a second diameter that is larger than the first diameter.

Regarding claim 14, Nakajima et al disclose the at least one adjustment mechanism (53) further comprises a hold-down screw (stopper screw 53b) extending generally co-axially through the adjusting screw (53a) and being adapted to tighten into a corresponding hole in the head stage (17) to retain the first plate (21) on the head stage (17).

Regarding claim 15, Nakajima et al disclose a method for testing semiconductor wafers (semiconductor wafer 14) using a probe station (probe apparatus 11) having a head stage (head plate 17), the method comprising: mounting an adapter member (ring plate 18) to an upper surface of the head stage (17); positioning a probe-card assembly (probe card holder 25 with probe card 22) in an aperture defined in a docking-equipment mounting member (hinge

mechanism 52) having docking equipment mounted thereon; and coupling the docking-equipment-mounting member (52) to the adapter member (18).

Regarding claim 16, Nakajima et al disclose positioning a semiconductor wafer (14) in the probe station (11), docking a tester (tester 28) to the first docking equipment; and testing the semiconductor wafer (14).

Regarding claim 23, Nakajima et al disclose adjusting [via adjustment screw mechanism 53] the tilt orientation of the probe-card assembly (25 with 22) relative to the head stage (17) to planarize the probe-card assembly (25 with 22) relative to a wafer chuck (wafer chuck 15) of the probe station (11).

Regarding claim 24, Nakajima et al disclose adjusting [via adjustment screw mechanism 53] the tilt orientation of the probe-card assembly (25 with 22) comprises adjusting the tilt orientation of the adapter member (18) relative to the head stage (17), thereby adjusting the tilt orientation of the docking-equipment-mounting member (52) and the probe-card assembly (25 with 22).

Regarding claim 25, Nakajima et al disclose adjusting [via adjustment screw mechanism 53] the tilt orientation of the probe-card assembly (25 with 22) comprises adjusting the tilt orientation of the first docking-equipment-mounting member (52) with respect to the adapter member (18) and the head stage (17), thereby adjusting the tilt orientation of the probe-card assembly (25 with 22).

Regarding claim 26, Nakajima et al disclose adjusting [via adjustment screw mechanism 53] the tilt orientation of the probe-card assembly (25 with 22) comprises rotating an adjusting screw (screw 53a) extending through the adapter member (18) and contacting the head stage (17)

to cause the adapter member (18), and therefore the docking-equipment-mounting member (52) and the probe-card assembly (25 with 22), to tilt relative to the head stage (17).

Regarding claim 27, Nakajima et al disclose coupling the docking-equipment-mounting member (52) to the adapter member (18) comprises aligning at least one alignment item on the docking-equipment-mounting member (52) with at least one corresponding alignment item on the adapter member (18).

Regarding claim 28, Nakajima et al disclose a method for testing semiconductor wafers (wafer 14) using a probe station (probe apparatus 11) having a head stage (head plate 17), the method comprising: coupling a probe-card-support device (probe unit 21) to an upper surface of the head stage (17); supporting a probe-card assembly (probe card holder 25 with probe card 22) with the probe-card-support device (21); positioning a semiconductor wafer (14) in the probe station (11); and adjusting [via adjusting screw mechanism 53] the tilt orientation of the probe-card-support device (21) with respect to the head stage (17), thereby adjusting the tilt orientation of the probe-card assembly (25 with 22) relative to the wafer (14) to optimize contact between probes (probes 23) of the probe-card assembly (25 with 22) and corresponding contacts of the wafer (14).

Regarding claim 29, Nakajima et al disclose docking a tester (tester 28) to the probe station (11); electrically connecting a probe card (probe card 22) of the probe-card assembly (25 with 22) to the wafer (14) and the tester 28), and testing the wafer (14).

Regarding claim 30, Nakajima et al disclose mounting docking equipment to the probe-card-support device (21), docking a tester (28) to the docking equipment, electrically connecting

a probe card (22) of the probe-card assembly (25 with 22) to the wafer (14) and the tester (28); and testing the wafer (14).

Regarding claim 31, Nakajima et al disclose the probe-card-support device (21) comprises a first plate and a second plate nested within the first plate, and supporting a probe-card assembly (25 with 22) with the probe-card-support device (21) comprises supporting the probe-card assembly (25 with 22) within an aperture defined in the second plate.

Regarding claim 32, Nakajima et al disclose providing at least one adjusting screw (adjusting screw 53a) extending through the probe-card-support device (21) and bearing against the head stage (17); and wherein adjusting the tilt orientation of the probe-card-support device (21) comprises rotating the adjusting screw (53a) to cause the probe-card-support device (21), and therefore the probe-card assembly (25 with 22), to tilt relative to the head stage (17).

Regarding claim 33, Nakajima et al disclose retaining the probe-card-support device (21) to the head stage (17) by tightening a retaining screw (dial 53d) into the head stage (17), the retaining screw (53d) extending through the adjusting screw (53a).

Regarding claim 34, Nakajima et al disclose an apparatus for testing semiconductor wafers (wafer 14) with a probe station (probing apparatus 11) having a head stage (head plate 17), the apparatus comprising a probe-card-support device (probe unit 21) for supporting a probe-card assembly (probe card holder 25 with probe card 22) when testing a semiconductor wafer (14) with the probe station (11), the probe-card-support device (21) being configured to be mounted to and completely removable from the head stage (17), the probe-card-support device (21) being adjustable [via adjustment screw mechanism 53] for adjusting the tilt orientation of the probe-card assembly (25 with 22) with respect to the head stage (17) and the semiconductor

wafer (14) so as to planarize the probe-card assembly (25 with 22) relative to the semiconductor wafer (14).

Regarding claim 35, Nakajima et al disclose the probe-card-support device (21) comprises a first plate for supporting the probe-card assembly (25 with 22) and a second plate for supporting the first plate, the second plate being configured to be mounted to and completely removable from the head stage (17).

Regarding claim 36, Nakajima et al disclose docking equipment (hinge mechanism 52) mounted to the probe-card-support device (21), the docking equipment (52) adapted to facilitate docking of a tester (tester 28) to the probe station (11).

Regarding claim 37, Nakajima et al disclose providing at least one adjusting screw (adjusting screw 53a) extending through the probe-card-support device (21) and bearing against the head stage (17); and wherein adjusting the tilt orientation of the probe-card-support device (21) comprises rotating the adjusting screw (53a) to cause the probe-card-support device (21), and therefore the probe-card assembly (25 with 22), to tilt relative to the head stage (17).

Regarding claim 38, Nakajima et al disclose retaining the probe-card-support device (21) to the head stage (17) by tightening a retaining screw (dial 53d) into the head stage (17), the retaining screw (53d) extending through the adjusting screw (53a).

Regarding claim 39, Nakajima et al disclose the probe-card-support device (21) is supported directly on the head stage (17).

Regarding claim 40, Nakajima et al disclose [see Figs. 1 and 3] a system for testing semiconductor devices (semiconductor wafers 14), the system comprising: a probe station (probing apparatus 11) comprising a head stage (head plate 17); a tester (tester 28) for docking

with the probe station (11) during testing of a semiconductor device (14); an adapter member (ring plate 18) configured to be mounted to and completely removable from the head stage (17); a probe-card-support member (probe unit 21) configured to be mounted to and completely removable from the adapter member (18), the probe-card-support member (21) having first and second opposed major surfaces and a major aperture for receiving a probe-card assembly (probe card holder 25 with probe card 22); and docking equipment (hinge mechanism 52) mounted to one of the first and second major surfaces of the probe-card-support member (21), the docking equipment (52) being adapted to facilitate docking of the tester (28) to the probe station (11).

Regarding claim 42, Nakajima et al disclose the head stage (17) defines a major aperture; the adapter member (18) defines a major aperture; and wherein whenever the adapter member (18) is mounted to the head stage (17) and the probe-card-support member (21) is mounted to the adapter member (18), the major aperture of the probe-card-support member (21) at least partially overlaps with the major apertures of the head stage (17) and adapter member (18) to allow the probe-card assembly (25 with 22) to be electrically connected to a semiconductor device (14) in the probe station (11).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Parmenter (5068601), Nakajima (5489853 & 5642056), Lee et al (5644246), Obikane et al (5828225), Botka et al (5923180), Hembree et al (6078186), Orsillo (6408500 & 6741072 & 6813817 & 6839948), Hollman et al (6424141), and Cheng et al (6853205) disclose a method and apparatus for testing a semiconductor device using a probe station.

5. Claims 4-5, 7, 12-13, 17-22, and 41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claim 43 is allowed over the prior art.

7. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 4, the primary reason for the allowance of the claim is due to the docking equipment comprises docking units for mating with docking units on a tester. Since claim 5 depends from claim 4, it also has allowable subject matter.

Regarding claim 7, the primary reason for the allowance of the claim is due a lip portion of a second plate is formed with a plurality of circumferentially spaced bosses wherein each boss being formed with a threaded hole for receiving a fastener for retaining a probe card assembly.

Regarding claim 12, the primary reason for the allowance of the claim is due docking equipment is mounted to a third plate. Since claim 13 depends from claim 12, it also has allowable subject matter.

Regarding claim 17, the primary reason for the allowance of the claim is due the docking equipment comprises a second docking equipment-mounting member coupled to an adapter member. Since claims 18-22 depend from claim 17, they also have allowable subject matter.

Regarding claim 43, the primary reason for the allowance of the claim is due the docking equipment comprises a second docking equipment-mounting member coupled to an adapter member.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Patent Examiner
Art Unit 2829

JMH
June 7, 2005